1 Digital Audio Interface

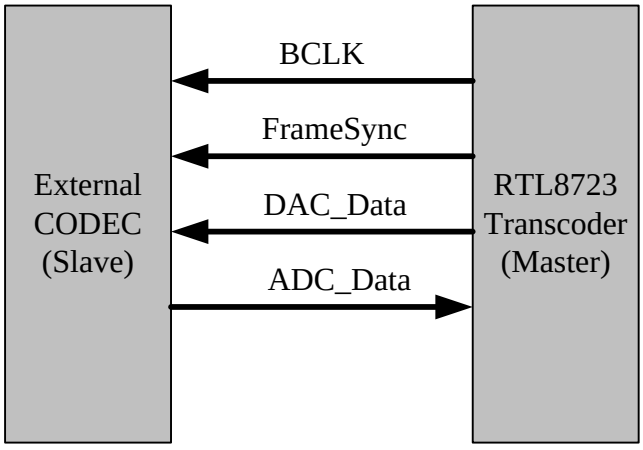
RTL8723 supports PCM digital audio interface used for transmitting digital audio/voice data to/from Audio Codec. There are features supported by RTL8723:

- Support both Master and Slave mode
- Programmable long/short Frame Sync
- Programmable MSB/LSB bit latch time(1st or 2nd BCLK)
- Programmable BCLK rising/falling edge trigger for latching data bits
- Support 8-bit a-Law/u-Law and 13/16-bit linear PCM formats
- Support maximum 4 slots in a frame.
- Support sign-extension and zero-padding for 8-bit and 13-bit samples
- Support padding of Audio Gain to 13-bit samples
- Programmable MSB/LSB first
- PCM Master clock output: 64, 128, 256 or 512kHz
- Support one SCO/ESCO link only

1.1 Master and Slave mode

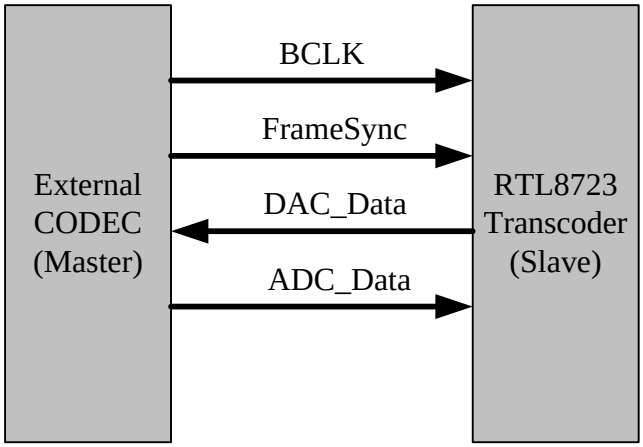
RTL8723 can be configured as either master or slave mode. As master mode, the RTL8723 generate BCLK and FrameSync, thus controls the data transfer over DAC_Data and ADC_Data. RTL8723 supports audio sample rate 8kHz(FrameSync), depends on the PCM data format and Multi-Slot operation, the clock output(BCLK) will be up to 512kHz.

- Master mode



In slave mode, RTL8723 responds with DAC_Data and ADC_Data to BCLK and FrameSync it receives from Audio Codec. RTL8723 can receive audio sample rate 8kHz(FrameSync), depends on the PCM data format and Multi-Slot operation, the clock input(BCLK) accepted will be up to 512kHz.

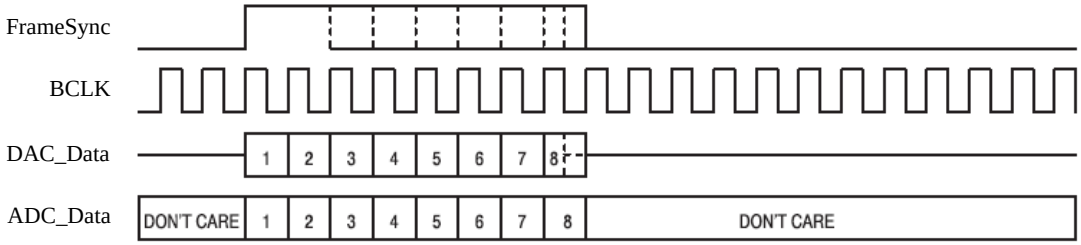
- Slave mode



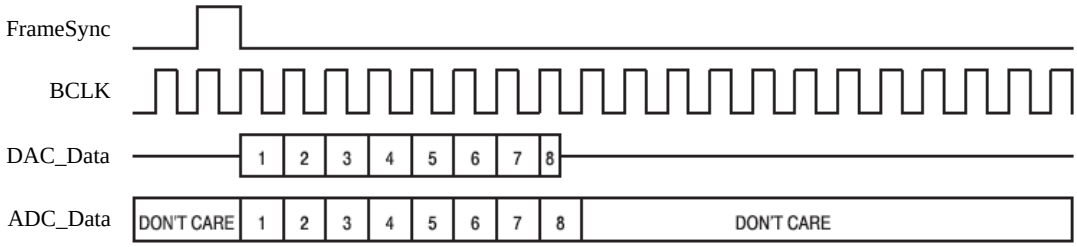
1.2 Programmable Long/Short Frame Sync

Frame Sync is the synchronizing function used to control the transfer of DAC_Data and ADC_Data. In common Audio Codec, Long Frame Sync indicates the start of ADC_Data at rising edge of FrameSync and Short Frame Sync indicates the start of ADC_Data at falling edge of FrameSync. Because there has no strict definition of how many BLCK clock should Long Frame Sync hold HIGH, RTL8723 has flexible options to set holding clock the Long Frame Sync should be to fit all possibility.

- Long Frame Sync



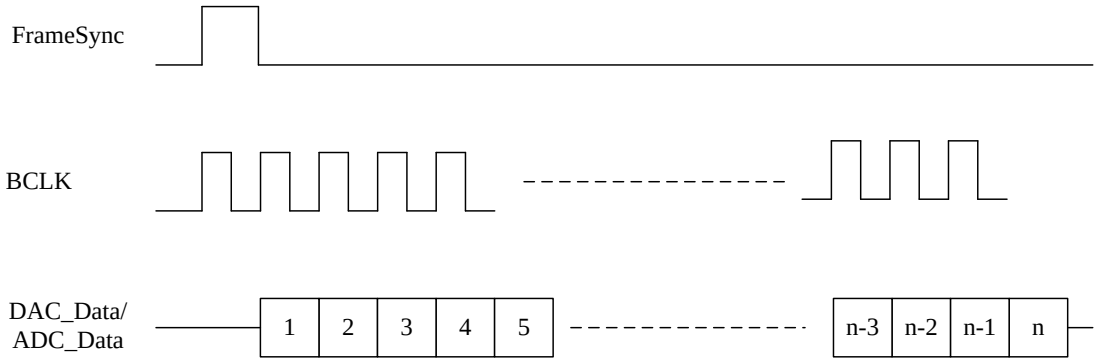
- Short Frame Sync



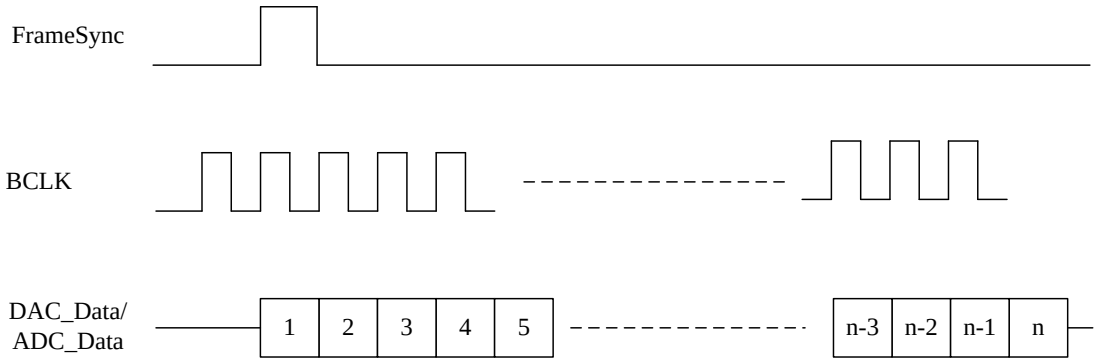
1.3 Programmable MSB/LSB bit latch time(1st or 2nd BCLK)

For compatibility with most Audio Codec, RTL8723 has options to set when the first bit will be latched or driven after FrameSync is driven high.

- Latched/Driven at 2nd BCLK



- Latched/Driven at 1st BCLK



1.4 Programmable BCLK rising/falling edge trigger for latching data bits

For compatibility with most Audio Codec, RTL8723 has options to set data latch/data drive phase.

1.5 8-bit a-Law/u-Law and 13/16-bit linear PCM formats

For mostly compatible with most Audio Codec, RTL8723 support 8-bit a-Law/u-Law and 8-bit, 13-bit, or 16-bit linear PCM sample formats.

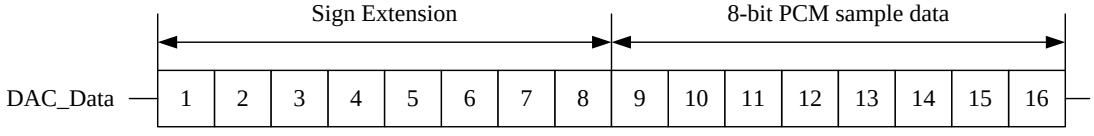
1.6 Maximum 4 slots in a frame

Multi-slot operation is supported with one SCO link.

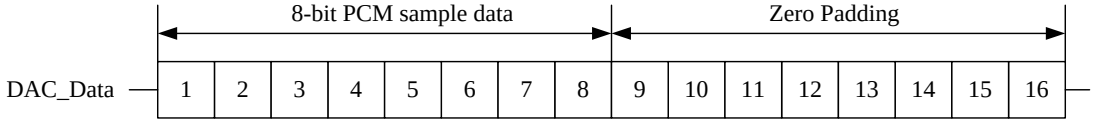
1.7 Sign-extension and zero-padding for 8-bit and 13-bit samples

For 16-bit linear PCM output format,, 3 or 8 unused bits maybe filled with sign extension, padding with zeros.

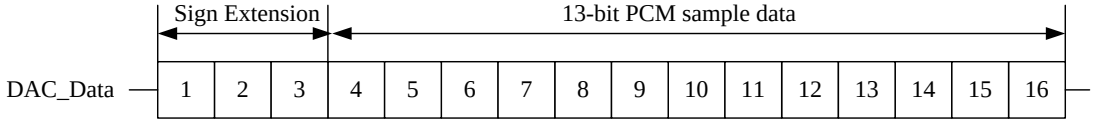
- 16-bit output data with 8-bit PCM sample data and Sign extension



- 16-bit output data with 8-bit PCM sample data and Zero padding



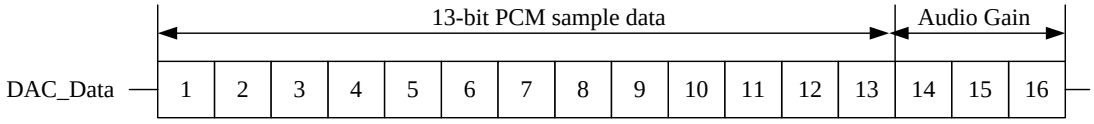
- 16-bit output data with 13-bit PCM sample data and Sign extension



1.8 Padding of Audio Gain to 13-bit samples

For 16-bit linear PCM output format, 3-bit programmable audio gain value can be padded to 13-bit sample data

- 16-bit output data with 13-bit PCM sample data and Audio gain



1.9 Programmable MSB/LSB first

For mostly compatible with most Audio Codec, RTL8723 support PCM data output/input with MSB/LSB as first bit..

1.10 PCM Master clock output: 64, 128, 256 or 512kHz

RTL8723 supports audio sample rate 8kHz(FrameSync), depends on the PCM data format and Multi-Slot operation, in Master mode the clock output(BCLK) will be 64, 128, 256, 512kHz.

1.11 one SCO/ESCO link only

One SCO/ESCO link is supported in RTL8723 to connect over PCM interface.

2 PCM Timming Information

- **PCM Interface**

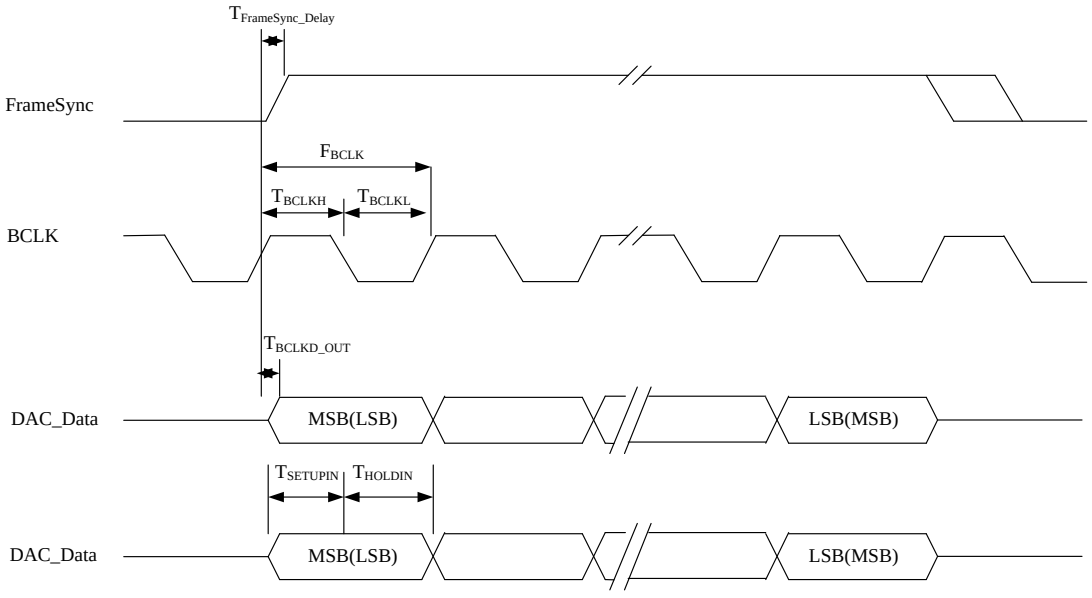
Symbol	Description	Min.	Typ.	Max.	Unit
F_{BCLK}	Frequency of BCLK(Master)	64	-	512	kHz
$F_{FrameSync}$	Frequency of FrameSync(Master)		8		kHz

F_{BCLK}	Frequency of BCLK(Slave)	64	-	512	kHz
$F_{FrameSync}$	Frequency of FrameSync(Slave)		8		kHz
D	Data size	8	8	16	bits
N	Number of slots per frame	1	1	1	

- **PCM Interface timing**

Symbol	Description	Min.	Typ.	Max.	Unit
T_{BCLKH}	High period of BCLK	980	-	-	ns
T_{BCLKL}	Low period of BCLK	970	-	-	ns
$T_{FrameSync\_Delay}$	Delay time from BCLK high to FrameSync high	-	-	75	ns
T_{BCLKD_OUT}	Delay time from BCLK high to valid DAC_Data	-	-	125	ns
$T_{SETUPIN}$	Set-up time for ADC_Data valid to BCLK low	10	-	-	ns
T_{HOLDIN}	Hold time for BCLK low to ADC_Data invalid	125	-	-	ns

- **PCM Interface(Long FrameSync)**



● PCM Interface(Short FrameSync)